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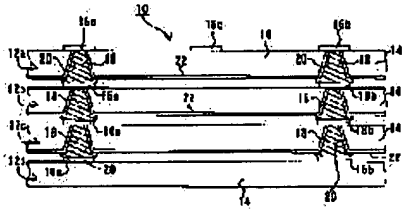
(54) SEMICONDUCTOR DEVICE AND MANUFACTURE THEREOF

(57)Abstract:
PROBLEM TO BE SOLVED: To enable semiconductor chips to be electrically interconnected with each other without the use of wires.
SOLUTION: A semiconductor device 10 is composed of semiconductor chips 12 (12a to 12d), which are laminated, aligning their electrodes 16a and 16b with each other respectively. Connection holes 20 are provided to the semiconductor chips 12a to 12c penetrating through semiconductor boards 14 so as to reach to the undersides of the electrodes 16a and 16b, and the electrodes 16a and 16b of the semiconductor chips 12 adjacent to each other in the vertical direction are mutually connected with each other with solder 18 filled into the connection holes 20.



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CLAIMS

[Claim(s)]
[Claim 1] The semiconductor device characterized by joining each aforementioned semiconductor chip mutually by the electric conduction material with which the hole which penetrated and formed the semiconductor substrate of the electrode section of each aforementioned semiconductor chip and the corresponding portion in the semiconductor device which has carried out two or more laminatings of the semiconductor chip in which the element was formed was filled up.
[Claim 2] The aforementioned electric conduction material is a semiconductor device according to claim 1 characterized by being solder or a low melting point metal.
[Claim 3] The aforementioned electric conduction material is a semiconductor device according to claim 1 characterized by being an electroconductive glue.
[Claim 4] It is the semiconductor device characterized by having connected mutually electrically by the electric conduction material arranged in the through hole in which each aforementioned semiconductor chip made the electrode section correspond, and had carried out the laminating, and these electrode sections penetrated the electrode section and the semiconductor substrate in the semiconductor device which carried out two or more laminatings of the semiconductor chip in which the element was formed, and prepared.
[Claim 5] The aforementioned electric conduction material is a semiconductor device according to claim 4 characterized by being the conductive film formed in the wall surface of the aforementioned through hole.
[Claim 6] The aforementioned electric conduction material is a semiconductor device according to claim 4 characterized by being the electroconductive glue with which the aforementioned through hole was filled up.
[Claim 7] The aforementioned electroconductive glue is a semiconductor device according to claim 6 characterized by being filled up with the opening in which the protective coat on the aforementioned electrode section of the aforementioned semiconductor chip located below was removed and formed.
[Claim 8] The aforementioned semiconductor chip which is equipped with the following and located below is the semiconductor device which carried out the laminating of the plurality of the semiconductor chip in which the element was formed characterized by what is electrically connected to the aforementioned electrode section of the aforementioned semiconductor chip in which the aforementioned electrode section is located up through the aforementioned bump. For the aforementioned semiconductor chip which the electrode section is made to correspond, has carried out the laminating, and is located up, each aforementioned semiconductor chip is the through hole formed in the semiconductor substrate of the portion corresponding to the aforementioned electrode section. The bump who penetrated and formed the aforementioned electrode section.
[Claim 9] The aforementioned electrode section of the semiconductor chip located in the aforementioned lower part and the aforementioned bump of a semiconductor chip located in the aforementioned upper part are a semiconductor device according to claim 8 characterized by having joined by the electroconductive glue.
[Claim 10] The manufacture method of the semiconductor device characterized by to have the polar zone of the semiconductor chip in_which the element was formed, the process which forms a through hole in the semiconductor substrate of the corresponding portion, the process which the aforementioned through hole is covered, and electric-conduction material heaps up, and forms the section, and the process which joins each aforementioned semiconductor chip mutually while carrying out the laminating of the plurality of the aforementioned semiconductor chip which has arranged the aforementioned electric-conduction material and connecting the aforementioned polar zone mutually electrically.
[Claim 11] The aforementioned electric conduction material is a soldering paste. the aforementioned peak raising section The process which covers the aforementioned through hole and arranges many soldering pastes from the capacity of a hole, The aforementioned semiconductor chip which has arranged the soldering paste is heated, a soldering paste is fused, and it forms according to the process which removes the flux in a soldering paste. the aforementioned junction The manufacture method of the semiconductor device according to claim 10 characterized by what is performed by fusing the solder which heated two or more aforementioned semiconductor chips which carried out the laminating, and has been arranged at the aforementioned through hole.
[Claim 12] It is the manufacture method of the semiconductor device according to claim 10 which the aforementioned electric conduction material is a low melting point metal, and is characterized by performing the aforementioned junction by heating and pressurizing the aforementioned low melting point metal of two or more semiconductor chips which carried out the laminating.
[Claim 13] The manufacture method of the semiconductor device characterized by to have the process which forms the through hole which penetrated the process which the polar zone which defined beforehand the plurality of the semiconductor wafer

in_which the element was formed, or a semiconductor chip is made to correspond, and carries out a laminating, and the aforementioned polar zone and the semiconductor substrate of the aforementioned semiconductor wafer or the semiconductor chip which carried out the laminating, and the process which prepares electric-conduction material in the aforementioned through hole, and connects the aforementioned polar zone mutually electrically.

[Claim 14] The electrical installation of the aforementioned polar zone is the manufacture method of the semiconductor device according to claim 13 characterized by carrying out to the wall surface of the aforementioned through hole by forming a metal membrane by vacuum evaporationo or plating.

[Claim 15] It is the manufacture method of the semiconductor device according to claim 13 characterized by removing a part of protective coat currently formed on the aforementioned polar zone, and for a part of aforementioned polar zone [at least] having exposed each aforementioned semiconductor wafer or the aforementioned semiconductor chip, and carrying out by injecting an electroconductive glue into the opening which the electrical installation of each aforementioned polar zone removed the aforementioned through hole and the aforementioned protective coat, and was formed.

[Claim 16] The manufacture method of a semiconductor device characterized by providing the following. Polar zone of the 1st semiconductor chip. The process which forms the through hole which penetrated the semiconductor substrate corresponding to this polar zone. The process which forms the bump who penetrated the polar zone through the through hole formed in the aforementioned polar zone. The process which arranges the 2nd semiconductor chip in piles and connects electrically the polar zone of the 2nd semiconductor chip of the above to the non-activity side side of the 1st semiconductor chip of the above through the aforementioned bump at the aforementioned polar zone of the 1st semiconductor chip of the above.

[Claim 17] The manufacture method of a semiconductor device according to claim 16 characterized by providing the following. The process which connects electrically the polar zone of the 1st semiconductor chip of the above and the 2nd semiconductor chip of the above is a process which arranges an electroconductive glue in the through hole formed in the semiconductor substrate of the 1st semiconductor chip of the above, and on the aforementioned polar zone of the 2nd semiconductor chip of the above. The process which arranges and puts the 2nd semiconductor device of the above on the non-activity side side of the 1st semiconductor chip, and joins the polar zone and the aforementioned bump of the 2nd semiconductor chip of the above by the aforementioned electroconductive glue.

[Translation done.]

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DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[The technical field to which invention belongs] this invention relates to the stacked MCP semiconductor device which was applied to the so-called multi chip package (MCP) which has two or more semiconductor chips, especially carried out the laminating of two or more semiconductor chips, and its manufacture method.
[0002]
[Description of the Prior Art] Advanced features and a miniaturization of a semiconductor device are attained by arranging two or more semiconductor chips and a multi chip package taking in recent years into one package, with highly-efficient-izing of electronic equipment, and a miniaturization. And there are what put two or more semiconductor chips in order superficially, and a thing which carried out the laminating of two or more semiconductor chips in the thickness direction in a multi chip package. Since the multi chip package which put the semiconductor chip in order superficially needs a latus component-side product, its contribution to the miniaturization of electronic equipment is small. For this reason, development stacked [MCP] which carried out the laminating of the semiconductor chip is performed briskly.
[0003]
[Problem(s) to be Solved by the Invention] When connecting mutually the semiconductor chip which carried out the laminating electrically as indicated by JP,6-37250,A, conventional stacked one MCP formed the terminal area in the periphery section of each semiconductor chip, and has connected between the terminals of each chip with the wire. For this reason, the semiconductor chip which carries out a laminating must make size small, so that it goes upwards, and the electrical installation between semiconductor chips not only becomes complicated, but accumulation efficiency and mounting efficiency fall. Moreover, when the degree of integration of a semiconductor chip improves, there is a possibility of the interval between wires becoming small and producing a short circuit between wires. Furthermore, in conventional stacked one MCP, it is made to join mutually the semiconductor chip which carried out the laminating with adhesives, the application of adhesives etc. is needed, and a process becomes complicated.
[0004] this invention was not made in order to cancel the fault of the aforementioned conventional technology, and it aims at connecting electrically mutually the semiconductor chip which carried out the laminating, without using a wire.
[0005] Moreover, this invention aims at joining mutually the semiconductor chip which carried out the laminating, without using adhesives.
[0006]
[Means for Solving the Problem] The 1st semiconductor device applied to this invention in order to attain the above-mentioned purpose is characterized by joining each aforementioned semiconductor chip mutually in the semiconductor device which has carried out two or more laminatings of the semiconductor chip in which the element was formed by the electric conduction material with which the hole which penetrated and formed the semiconductor substrate of the polar zone of each aforementioned semiconductor chip and the corresponding portion was filled up.
[0007] Thus, by leaving the polar zone, forming a through hole in a semiconductor substrate, and joining the polar zone of each semiconductor chip by the electric conduction material with which this through hole was filled up, the semiconductor device concerning the 1st of the constituted this invention can connect each semiconductor chip electrically, without using a wire, and can join each semiconductor chip mutually.
[0008] If solder or a low melting point metal is used as electric conduction material, while being able to make the electric resistance by junction small, the big junction force is acquired. Moreover, if an electroconductive glue is used as electric conduction material, since heating is not needed, simplification of a process can be attained and the damage by heat, such as an element, etc. can be avoided.
[0009] And in the semiconductor device with which the semiconductor device concerning the 2nd of this invention carried out two or more laminatings of the semiconductor chip in which the element was formed, it is characterized by having connected mutually electrically by the electric conduction material arranged in the through hole in which each aforementioned semiconductor chip makes the polar zone correspond, and has carried out the laminating, and these polar zone penetrated and prepared the polar zone and the semiconductor substrate.
[0010] Thus, also in the semiconductor device concerning the 2nd of the constituted this invention, each semiconductor chip can be connected electrically, without using a wire. Moreover, since the through hole which penetrated the polar zone and the semiconductor substrate is formed, it is possible to bundle up, where the laminating of each semiconductor chip is carried out,

and to form a through hole, and simplification of a process can be attained.
[0011] Electric conduction material may be the conductive film formed in the wall surface of a through hole. This conductive film can be formed by depositing the film of conductive metals, such as copper and aluminum, by vacuum evaporationo or plating. Furthermore, each semiconductor chip is mutually joinable by making a through hole fill up with and harden this electroconductive glue, using an electroconductive glue as electric conduction material. And while the touch area of the polar zone of each semiconductor chip and an electroconductive glue increases and being able to make electrical installation more reliable by filling up with an electroconductive glue the opening in which the protective coat on the polar zone of the semiconductor chip located caudad was removed and formed, the junction force between each semiconductor chip can be enlarged.
[0012] In the semiconductor device with which the semiconductor device concerning the 3rd of this invention carried out the laminating of the plurality of the semiconductor chip in which the element was formed moreover, each aforementioned semiconductor chip The aforementioned semiconductor chip which the polar zone is made to correspond, has carried out the laminating, and is located up The aforementioned semiconductor chip which has the through hole formed in the semiconductor substrate of the portion corresponding to the aforementioned polar zone and the bump who penetrated and formed the aforementioned polar zone, and is located caudad The aforementioned polar zone is characterized by what is electrically connected to the aforementioned polar zone of the aforementioned semiconductor chip located up through the aforementioned bump.
[0013] Thus, each semiconductor chip can be connected electrically, without using a wire also in the constituted this invention. And if the electrode section of the semiconductor chip located below and the bump of a semiconductor chip located in the upper part are joined by the electroconductive glue, while electric connection can carry out more certainly, each semiconductor chip is mutually joinable.
[0014] The electrode section of the semiconductor chip in which the 1st formed the element of the method of manufacturing the above-mentioned semiconductor device, and the process which forms a through hole in the semiconductor substrate of the corresponding portion, It is characterized by having the process which the aforementioned through hole is covered, and electric conduction material heaps up, and forms the section, and the process which joins each aforementioned semiconductor chip mutually while carrying out the laminating of the plurality of the aforementioned semiconductor chip which has arranged the aforementioned electric conduction material and connecting the aforementioned electrode section mutually electrically. The semiconductor device concerning the 1st of this invention is obtained by this, and while being able to connect mutually electrically, without carrying out wirebonding of between semiconductor chips, the semiconductor chips which carried out the laminating are joinable.
[0015] Electric conduction material may be a soldering paste. In this case, it can heap up, and can form according to the process which the section covers a through hole and arranges many soldering pastes from the capacity of a hole, and the process which heats the semiconductor chip which has arranged the soldering paste, fuses a soldering paste, and removes the flux in a soldering paste, and junction can be performed by fusing the solder which heated two or more semiconductor chips which carried out the laminating, and has been arranged at the through hole. Namely, if a soldering paste is used, the laminating of the semiconductor chip will be carried out, solder can be performed and solder can join each semiconductor chip automatically with the self-weight of a semiconductor chip heating and by carrying out a reflow at the time of ******. Moreover, when a low melting point metal is used as electric conduction material, if junction is performed by heating and pressurizing the low melting point metal of two or more semiconductor chips which carried out the laminating, it can ensure junction between the electrode sections, and junction between semiconductor chips. And it becomes possible by using low melting point metals, such as tin and silver, to realize a lead free-lancer.
[0016] The manufacture method of the 2nd semiconductor device concerning this invention The process which the electrode section which defined beforehand the plurality of the semiconductor wafer in which the element was formed, or a semiconductor chip is made to correspond, and carries out a laminating, It is characterized by having the process which forms the through hole which penetrated the aforementioned electrode section and the semiconductor substrate of the aforementioned semiconductor wafer or semiconductor chip which carried out the laminating, and the process which prepares electric conduction material in the aforementioned through hole, and connects the aforementioned electrode section mutually electrically. Thereby, the semiconductor device concerning the 2nd of this invention can be obtained.
[0017] The electrical installation of the electrode section can form a metal membrane in the wall surface of a through hole by vacuum evaporationo or plating, and can perform it on it. Moreover, when a part of protective coat currently formed on the electrode section is removed and a part of electrode section [at least] has exposed each semiconductor wafer or the semiconductor chip, the electrical installation of each electrode section injects an electroconductive glue into the opening which removed the through hole and the protective coat and was formed, and performs it. Thereby, the touch area of the electrode section and an electroconductive glue can become large, can ensure electrical installation, and can increase the bonding strength between each semiconductor chip.
[0018] The manufacture method of the semiconductor device concerning the 3rd of this invention The process which forms the through hole which penetrated the semiconductor substrate corresponding to the 1st electrode section and this electrode section of a semiconductor chip, The process which forms the bump who penetrated the electrode section through the through hole formed in the aforementioned electrode section, It is characterized by having the process which arranges the 2nd semiconductor chip in piles and connects electrically the electrode section of the 2nd semiconductor chip of the above to the non-activity side side of the 1st semiconductor chip of the above through the aforementioned bump at the aforementioned electrode section of the

1st semiconductor chip of the above. Thereby, the semiconductor device concerning the 3rd of this invention can be obtained.
[0019] And the process which arranges an electroconductive glue in the through hole which formed in the semiconductor substrate of the 1st semiconductor chip the process which connects electrically the electrode section of the 1st semiconductor chip and the 2nd semiconductor chip, and on the electrode section of the 2nd semiconductor chip, By arranging and putting the 2nd semiconductor device on the non-activity side side of the 1st semiconductor chip, looking like [the process joined by the electroconductive glue] the 2nd electrode section and bump of a semiconductor chip, and therefore performing them The certainty of electrical installation can be improved and it becomes joinable [semiconductor chips].
[0020]
[Embodiments of the Invention] The form of desirable operation of the semiconductor device concerning this invention and its manufacture method is explained in detail according to an accompanying drawing.
[0021] some semiconductor devices which drawing 1 requires for the form of the 1st operation of this invention -- it is a cross section In drawing 1 , as for the semiconductor device 10 which constitutes the stacked mold MCP, the laminating of the semiconductor chip 12 (12a-12d) of plurality (in the case of an operation form four) has been carried out. And each semiconductor chip 12 has the semiconductor substrate 14 which consists of silicon, and while having formed elements, such as a transistor which is not illustrated in the upper part of the semiconductor substrate 14, and resistance, a capacitor, the electrode section 16 is formed. These electrode sections 16 are formed by electric conduction material, such as aluminum and an aluminium alloy, and are electrically connected to elements, such as a transistor, through the wiring (not shown) formed in the semiconductor substrate 14.
[0022] Each semiconductor chip 12 makes the electrode sections 16a and 16b defined beforehand correspond, has carried out the laminating, and is electrically connected mutually with the solder 18 whose electrode sections 16a and 16b which the adjoining semiconductor chip 12 made correspond are electric conduction material.
[0023] That is, the catching hole (through hole) 20 which penetrated and formed the semiconductor substrate 14 in the electrode sections 16a and 16b of the semiconductor substrate 14 and the corresponding portion is formed in other semiconductor chips 12a-12c except 12d of semiconductor chips of a bottom. These catching holes 20 are gradually extended towards a non-activity side side (undersurface side of drawing 1) from the side which formed the electrode section 16 which is the active side side of a semiconductor chip 12. And the insulator layer 22 which consists of 2 silicon oxides (SiO2) is formed, and it is made to have not flowed through the solder 18 and the semiconductor substrate 14 which have been arranged in a catching hole 20 directly electrically on the non-activity side of the semiconductor substrate 14, and the wall surface of a catching hole 20. Furthermore, the solder 18 arranged in the catching hole 20 of the semiconductor chip 12 located in the drawing bottom was projected from the non-activity side of the semiconductor substrate 14, and is joined to the upper surface of the electrode section 16 of the bottom semiconductor chip 12 which adjoins the non-activity side side while having joined to the undersurface of the electrode section 16.
[0024] thus, the connection whose each semiconductor chips [12a-12d] electrode sections 16a and 16b made to correspond formed the semiconductor device 10 concerning the formed 1st operation form in the semiconductor substrate 14 -- since the solder 18 prepared in the hole 20 connects directly electrically, the wire for connecting each semiconductor chip 12 electrically is not needed, but electrical installation between semiconductor chip 12 can be performed easily And in order not to use the wire which is easy to deform, even if it makes the interval between the electrode sections 16 small, generating of a short circuit etc. can be lost, and it becomes possible to improve the degree of integration of the element of each semiconductor chip 12. Moreover, since it is not necessary to form a terminal area in the periphery section of each semiconductor chip 12 which carried out the laminating, even if it makes [many] the number of laminatings of a semiconductor chip 12, it is not necessary to make small size of the semiconductor chip located up, and mounting efficiency can be raised.
[0025] Furthermore, a semiconductor device 10 can skip the process which joins a semiconductor chip mutually with adhesives by having joined the electrode section 16 of the semiconductor chip 12 which adjoins through solder 18. And in the form of operation, since the catching hole 20 formed in the semiconductor chip 12 is gradually extended towards the non-activity side side which joins other semiconductor chips, the junction force of solder 18 and the electrode section 16 (for example, electrode section 16 of the solder 18 of semiconductor chip 12a and semiconductor chip 12b) of other semiconductor chips can be enlarged.
[0026] in addition, the electrode section 16 of semiconductor chip 12a located in the best stage of drawing 1 when connecting a semiconductor device 10 to the substrate of a package electrically -- wirebonding -- it carries out by carrying out face down bonding
[0027] In the gestalt of the aforementioned implementation, although the case where electric conduction material was solder 18 was explained, electric conduction material may be the so-called low melting point metals, such as tin and silver, and may be electroconductive glues.
[0028] Drawing 2 forms the electrode section 16 and produces a semiconductor chip 12 while it forms wiring first after forming the element which shows the important section of process drawing explaining the manufacture method of the semiconductor device 10 concerning the form of the 1st operation and which is not illustrated to the semiconductor substrate 14 by the well-known method, as shown in drawing 2 (a). Then, from the rear-face (non-activity side) side of a semiconductor chip 12, wet etching is carried out and the catching hole 20 which penetrates the semiconductor substrate 14 and arrives at the rear face of the electrode section 16 is formed for the semiconductor substrate 14.
[0029] Next, as shown in drawing 2 (b), the insulator layer 22 which covers the non-activity side and catching hole 20 of the semiconductor substrate 14, and consists of diacid-ized silicon (SiO2) by the CVD using the tetrapod ethoxy silane (TEOS) etc.

is formed. Furthermore, an insulator layer 22 is covered, the photoresist film 30 is formed, by the photo lithography method, this is exposed and developed, and carries out patterning, a hole 32 is established in an electrode 16 and the corresponding position, and the insulator layer 22 currently formed in the field of the polar zone 16 is exposed.

[0030] Then, the insulator layer 22 to which it etched into by having considered as the mask, and the photoresist film 30 was exposed is removed (refer to drawing 2 (c)). Next, the soldering paste 34 used as electric conduction material is formed in a catching hole 20 using screen printing. in order that this soldering paste 34 may join to the polar zone of other semiconductor chips so that it may mention later -- from a catching hole 20 -- suitably -- ********** -- it prepares like Then, the semiconductor chip 12 which has arranged the soldering paste 34 is put into a reflow furnace, a soldering paste 34 is heated and flux is removed, and as shown in drawing 2 (d), it is made the solder plug 36.

[0031] Next, as shown in drawing 2 (e), the predetermined polar zone 16 is made to correspond, and as a non-activity side turns up, it accumulates the semiconductor chip 12 of the number of requests in which the solder connecting plug 36 was formed on it. And where two or more semiconductor chips 12 are accumulated, it arranges at a reflow furnace, and the solder plug 36 is heated to melting temperature. Thereby, the solder plug 36 is fused and is crushed by the weight of a semiconductor chip 12. Then, if a semiconductor chip 12 is cooled, the semiconductor device 10 which solder 18 connected mutually electrically, and the polar zone 16 of the semiconductor chip 12 of the adjoining upper and lower sides was joined to it with it, and was shown in drawing 1 can be obtained.

[0032] In addition, when the electric conduction material arranged to the catching hole 20 is low melting point metals, such as silver, the reflow process of drawing 2 (d) can be skipped. And when joining two or more piled-up semiconductor chips of each mutually with low melting point metals, such as silver, while heating the semiconductor chip 12 of a bottom in the best stage, or both, the whole semiconductor chip which carried out the laminating is pressurized in the vertical direction. Thereby, while being able to transmit heat to a low melting point metal easily through the semiconductor substrate 14, the polar zone of each semiconductor chip is certainly joinable to a low melting point metal. Furthermore, a heating process can be skipped when an electroconductive glue is used as electric conduction material.

[0033] some semiconductor devices which drawing 3 requires for the gestalt of the 2nd operation -- it is a cross section As for the semiconductor device 40 shown in drawing 3 (a), the laminating of the semiconductor chip 12 (12a-12c) of plurality (it sets in this operation gestalt and is three) has been carried out. Each semiconductor chip 12 is arranged so that an active side side may turn into the drawing 3 bottom, makes the polar zone 42 defined beforehand correspond, and has carried out the laminating. And the metal membrane 46 which is the electric conduction material which has formed the through hole 44 which penetrated the polar zone 42 and the semiconductor substrate 14 of each semiconductor chip 12, and formed the semiconductor device 40 in the wall surface of this through hole 44 by vacuum evaporationo, plating, etc. is formed, and the polar zone 42 of each semiconductor chip 12 is mutually connected electrically through the metal membrane 46. However, the insulator layers 45, such as a silicon oxide, are formed in the portion from which each semiconductor chip 12 serves as a wall surface of the through hole 44 of the semiconductor substrate 14, and a metal membrane 46, the semiconductor substrate 14, and between are intercepted electrically.

[0034] Thus, the formed semiconductor device 40 can be carried out like drawing 4 , and can be manufactured. First, as shown in Step 60 of drawing 4 , an element, the polar zone, etc. are formed in a semiconductor wafer by the usual method. Then, while turning into request number of sheets (it sets in this operation gestalt and they are three sheets) the semiconductor wafer in which the element etc. was formed and turning an active side up, the polar zone 42 which forms a through hole 44 is made to correspond, and a laminating is carried out (Step 62). Next, where the laminating of the semiconductor wafer is carried out, a laser beam etc. is used for the portion of the polar zone 42, and a through hole 44 is formed (Step 64). You may form this through hole 44 by etching. Moreover, after making a hole by the laser beam since the wall surface of a hole is ruined when forming a through hole 44 using a laser beam, to ********** and operate orthopedically is good.

[0035] Then, as shown in Step 66, an insulator layer 45 is formed in the portion used as the wall surface of the through hole 44 of the semiconductor substrate 14. Formation of this insulator layer 45 heats the semiconductor wafer in which the through hole 44 was formed, in being immersed and an oxidizing atmosphere in concentrated-nitric-acid liquid, oxidizes the through-hole wall surface section of the semiconductor substrate 14, and is SiO2. It carries out. Then, alkali etc. removes the metal oxide film (passive state) currently formed in the polar zone 42.

[0036] Next, as shown in Step 68, a metal membrane 46 is formed in the wall surface of the through hole 44 which formed the insulator layer by vacuum evaporationo, electroless deposition, etc. In addition, when forming a metal membrane 46 by plating, it is good to form ground metals, such as Ti (titanium), by vacuum deposition or CVD, and to form metal membranes, such as copper, by electroless deposition after that.

[0037] If a metal membrane 46 is formed in a through hole 44, it will divide into a chip size using a laser beam, a diamond blade, etc., carrying out the laminating of the semiconductor wafer, as shown in Step 70. Furthermore, the laminate cut to the chip size is mounted in the substrate of a package, a resin seal etc. is performed, and it is made the MCP semiconductor device of a stacked mold (Step 72).

[0038] In addition, after cutting the semiconductor wafer in which an element, the polar zone 42, etc. were formed and forming a semiconductor chip 12, the laminating of the semiconductor chip of the number of requests is carried out, and you may make it form a through hole 44 in the aforementioned operation gestalt, although the case where carried out the laminating of the semiconductor wafer and a through hole 44 was formed was explained.

[0039] drawing 3 (b) -- a part of modification of the 2nd operation gestalt -- it is a cross section Two semiconductor chips 12a and 12b double a non-activity side side, and the laminating of this semiconductor device 50 has been carried out. And the

through hole 44 which penetrated the polar zone 42 which each semiconductor chip 12 made correspond, and the semiconductor substrate 14 is formed, the metal membrane 46 is formed in the wall surface of this through hole 44, and the polar zone 42 of each semiconductor chip 12 is electrically connected by the metal membrane 46.
[0040] In addition, it is the same as that of the above to have insulated the wall surface of the through hole 44 of the semiconductor substrate 14 by the insulator layer 45. Moreover, this semiconductor device 50 can be manufactured almost like the case of a semiconductor device 40. Moreover, although the semiconductor device 50 shown in drawing 3 (b) explained the case where two semiconductor chips 12 were piled up, it can carry out the laminating of arbitrary numbers of the semiconductor chips among semiconductor chips 12a and 12b.
[0041] some semiconductor devices which drawing 5 requires for the gestalt of the 3rd operation -- it is a cross section As for the semiconductor device 74 shown in drawing 5 (a), the laminating of the semiconductor chip 76 (76a-76c) of plurality (in the case of an operation gestalt three) has been carried out. And the polar zone 78 and the semiconductor substrate 80 which were formed in each semiconductor chip 76 are penetrated, the through hole 82 is formed, this through hole 82 is filled up with the electroconductive glue 84 which is electric conduction material, it is joined by the electroconductive glue 84 and each semiconductor chip 76 is unified. Moreover, the opening 88 formed by exfoliating in the passivation film 86 as a protective coat which consists of a silicon oxide of the semiconductor chips 76b and 76c located down the drawing etc. is also filled up with the electroconductive glue 84.
[0042] That is, after a semiconductor chip generally forms wiring and the polar zone, it formed the passivation film 86 on it, and has protected wiring etc. And the passivation film 86 located on the polar zone 78 is removed in order to connect with other semiconductor chips, the polar zone of a package substrate, etc. electrically. For this reason, if two or more laminatings of the semiconductor chip are carried out, since the place which removed the passivation film 86 will serve as an opening 88, by filling up the opening 86 with an electroconductive glue 84, and performing electrical installation of each polar zone 78, the touch area of an electroconductive glue 84 and the polar zone 78 is increased, and more positive electrical installation is performed, and the junction force between each semiconductor chip is enlarged.
[0043] It manufactures by carrying out this semiconductor device 74 as following. First, etching etc. removes the passivation film 86 which exists on the polar zone 78 of the semiconductor wafer in which an element, the polar zone 78, etc. were formed, or a semiconductor chip 76, and the polar zone 78 is exposed. Next, the polar zone 78 is made to correspond and two or more laminatings of the semiconductor wafer or semiconductor chip to which the polar zone 78 was exposed are carried out. Then, in the state where the laminating of a semiconductor wafer or the semiconductor chip 76 was carried out, the through hole 82 which penetrated the polar zone 78 and the semiconductor substrate 80 of each semiconductor chip 76 is formed collectively, and the insulator layer which is not illustrated on the wall surface of the breakthrough 82 of the semiconductor substrate 80 is prepared. Although it can form like the gestalt of the 2nd operation of the above, you may form this insulator layer as follows.
[0044] The semiconductor wafer or semiconductor chip 76 which formed the through hole 82 where a laminating is carried out is put into a CVD system as it is, and a silicon oxide is formed in the wall surface of a through hole 82 by CVD using TEOS etc. At this time, as shown in drawing 6 (a), a silicon oxide 89 is deposited on the top semiconductor wafer or the upper surface of semiconductor chip 76a, and the wall surface of the breakthrough 82 of each semiconductor wafer or semiconductor chips 76a-76c, and is hardly formed in the field which forms the opening 88 formed between each semiconductor wafer or each semiconductor chip 76. Since the passivation film 86 is thin, this has the narrow width of face of the vertical direction of an opening 88, and since the circumference moreover serves as a letter object of sealing, it is because material gas is not supplied to the back of an opening 88.
[0045] Thus, if a silicon oxide 89 is formed, it will ********** extensively from the upper part of the semiconductor wafer with which the silicon oxide 89 was formed, or semiconductor chip 76a, and as shown in drawing 6 (b), the silicon oxide 89 formed by the upper surface of semiconductor wafer or semiconductor chip 76a will be removed. Thereby, the insulator layer which becomes the wall surface of a through hole 82 from a silicon oxide 89 is formed.
[0046] Next, while sealing the lower part of a through hole 82, pressing an electroconductive glue 84 fit from the upper part of a through hole 82 and filling up the interior of a through hole 82 and an opening 88 with an electroconductive glue 84, it is made to arrange and harden so that it may wear on the upper surface of the top electrode section 78. Then, if it is the semiconductor wafer which carried out the laminating to having described above similarly, it divides into a chip size and mounts in a package substrate.
[0047] Drawing 5 (b) shows the modification of the semiconductor device concerning the 3rd operation form. As for this semiconductor device 110, the laminating of the semiconductor chip 112 (112a-112c) has been carried out. The crevice 114 is formed in a part of active side of the semiconductor substrate 80, and, as for each semiconductor chip 112, the electrode section 116 is formed in this crevice 114. For this reason, an opening 118 will be formed in the upper part of the electrode section 116 of a lower semiconductor chip if the laminating of each semiconductor chip 112 is carried out. Moreover, the through hole 82 which penetrated the electrode section 116 and the semiconductor substrate 80 is formed in the center section of the crevice 114. The insulator layer which consists of a silicon oxide etc. and which is not illustrated is formed in the wall surface of this through hole 82. And while having filled up the through hole 82 and the opening 118 with the electroconductive glue 84 and having connected electrically the electrode section 116 of each semiconductor chip 112, the semiconductor chip 112 which adjoins in the vertical direction is joined mutually. The same effect as the above can be acquired also in the semiconductor device 110 of this modification.
[0048] some semiconductor devices which drawing 7 requires for the 4th operation gestalt -- it is a cross section Two semiconductor chips 76a and 76b make the polar zone 78 correspond, and the laminating of the semiconductor device 90 shown

in drawing 7 (a) has been carried out. And while having formed the through hole 92 of the shape of a taper gradually extended towards the bottom from which upper semiconductor chip 76a becomes the semiconductor substrate 80 of the lower part of the polar zone 78 a non-activity side side, the through hole 94 smaller than a through hole 92 is formed also in the polar zone 78. Moreover, the stud bump 96 who consists of gold is formed in the polar zone 78. This stud bump 96 has the connection 98 which projected from the soffit of the semiconductor substrate 80, contacted the upper surface of the polar zone 78 of semiconductor chip 76b which the soffit of a connection 98 arranges and fixed to the semiconductor chip 76a bottom, and is connecting electrically each polar zone 78 of both the semiconductor chips 76a and 76b while a part extends under the polar zone 78 through a through hole 94.

[0049] Thus, after the constituted semiconductor device 90 removes the passivation film 86 on the polar zone 78 of semiconductor chip 76a, it **********s the semiconductor substrate 80 and forms a through hole 92. Furthermore, the polar zone 78 of semiconductor chip 76a is **********ed, and a through hole 94 is formed. Then, the capillary tube of wirebonding equipment is arranged on the through hole 94 of the polar zone 78, and the stud bump 96 is formed, pulling out a golden wire. Thereby, as the stud bump 96 showed drawing 7 (a), it projects under the polar zone 78 and a connection 98 is formed. And if the polar zone 78 is made to correspond, semiconductor chips 76a and 76b are piled up and both are fixed with adhesives etc., it will be alike, and more, the stud bump's 96 connection 98 is contacted to the polar zone 78 of downward semiconductor chip 76b, and it connects electrically.

[0050] Drawing 7 (b) shows the modification of the 4th operation gestalt. As for this semiconductor device 100, through holes 92 and 94 are formed in the upper semiconductor substrate 80 and upper polar zone 78 of semiconductor chip 76a. Furthermore, the stud bump 96 is formed in the polar zone 78 at upper semiconductor chip 76a. This stud bump 96 is the connection 98 which the lower part penetrated the polar zone 78 and was projected under the polar zone 78. And the connection 98 is electrically connected to the polar zone 78 of lower semiconductor chip 76b through the electroconductive glue 102. Thus, while being able to make electrical installation more reliable by joining the lower polar zone 78 and the lower stud bump 96 of semiconductor chip 76b using an electroconductive glue 102, semiconductor chips 76a and 76b are mutually joinable. In addition, the insulator layer which is not illustrated is prepared in the wall surface of a through hole 92.

[0051] Thus, the semiconductor device 100 of constituted drawing 7 (b) forms the stud bump 96 in the polar zone 78 of semiconductor chip 76a used as the bottom like the above. A soffit projects and bends from the inferior surface of tongue of the semiconductor substrate 80, and this stat bump 96 makes it the size of a grade. Moreover, semiconductor chip 76b used as the bottom arranges the electroconductive glue 102 of optimum dose on the polar zone 78, after removing the passivation film 86 on the polar zone 78. And semiconductor chip 76a is arranged in piles on semiconductor chip 76b, and the polar zone 78 of both the semiconductor chips 76a and 76b is electrically connected through an electroconductive glue 102 and the stud bump 96.

[0052] Drawing 7 (c) shows other examples of the through hole formed in a semiconductor substrate. The active side side in which the polar zone 78 was formed serves as the straight hole 106 which has the wall surface which intersected perpendicularly with the field of the semiconductor substrate 80, and this through hole 104 serves as the expansion hole 108 which the non-activity side side of the semiconductor substrate 80 extended gradually towards the non-activity side.

[0053] Thus, if the through hole 104 of the shape of a funnel which consists of a straight hole 106 and an expansion hole 108 is formed, when the semiconductor substrate 80 is thick, it can prevent opening in the non-activity side of a through hole 104 becoming larger than required, and risk (it connects) of contacting the polar zone of an upper semiconductor chip and the polar zone which adjoined the polar zone of a corresponding bottom semiconductor chip can be avoided. Furthermore, when the polar zone 78 approaches and is prepared, it can prevent that the adjoining through holes are connected on the way. Moreover, as for the funnel-like through hole 104, when filled up with electric conduction material, the whole can lessen the fill of electric conduction material as compared with the through hole currently formed in the shape of a taper. And when carrying out the laminating of the semiconductor chip in which bumps, such as a stud bump, were formed on the polar zone 78, the alignment of a bump and a through hole, i.e., the alignment of a semiconductor chip which carries out a laminating, can be performed easily.

[0054] This through hole 104 can be formed as follows.

[0055] First, wet etching of the semiconductor substrate 80 is carried out from a non-activity side side, and the expansion pore 108 is formed. If predetermined-time etching is carried out and the expansion pore 108 is formed, a semiconductor chip 76 will be washed, it will dry, a laser beam will be irradiated from a non-activity side side, and the straight hole 106 will be formed. In addition, after forming the straight hole 106, you may perform the plastic surgery which carries out wet etching and smooths the wall surface of a through hole 104. Moreover, the through hole 94 of the polar zone 78 is formed like the above. And you may form a parallel bore 106 by the dry etching which used plasma. Furthermore, the parallel bore 106 which penetrated the body substrate 80 first is formed by the laser beam or plasma etching, and you may make it form the expansion hole 108 by wet etching after that.

[0056]

[Effect of the Invention] The mounting efficiency of a package can be raised [as explained above, while according to this invention the semiconductor chip which carried out the laminating, without using a wire can be connected mutually electrically and electrical installation becomes easy,] so that a laminating is carried out, and a semiconductor chip may not be made small. Moreover, a semiconductor chip can be mutually joined by joining the polar zone by electric conduction material, without using adhesives.

[Translation done.]

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TECHNICAL FIELD

[The technical field to which invention belongs] this invention relates to the stacked MCP semiconductor device which was applied to the so-called multi chip package (MCP) which has two or more semiconductor chips, especially carried out the laminating of two or more semiconductor chips, and its manufacture method.

[Translation done.]

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EFFECT OF THE INVENTION

[Effect of the Invention] The mounting efficiency of a package can be raised [as explained above, while according to this invention the semiconductor chip which carried out the laminating, without using a wire can be connected mutually electrically and electrical installation becomes easy,] so that a laminating is carried out, and a semiconductor chip may not be made small. Moreover, a semiconductor chip can be mutually joined by joining the electrode section by electric conduction material, without using adhesives.

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TECHNICAL PROBLEM

[Problem(s) to be Solved by the Invention] When connecting mutually the semiconductor chip which carried out the laminating electrically as indicated by JP,6-37250,A, conventional stacked one MCP formed the terminal area in the periphery section of each semiconductor chip, and has connected between the terminals of each chip with the wire. For this reason, the semiconductor chip which carries out a laminating must make size small, so that it goes upwards, and the electrical installation between semiconductor chips not only becomes complicated, but accumulation efficiency and mounting efficiency fall. Moreover, when the degree of integration of a semiconductor chip improves, there is a possibility of the interval between wires becoming small and producing a short circuit between wires. Furthermore, in conventional stacked one MCP, it is made to join mutually the semiconductor chip which carried out the laminating with adhesives, the application of adhesives etc. is needed, and a process becomes complicated.

[0004] this invention was not made in order to cancel the fault of the aforementioned conventional technology, and it aims at connecting electrically mutually the semiconductor chip which carried out the laminating, without using a wire.

[0005] Moreover, this invention aims at joining mutually the semiconductor chip which carried out the laminating, without using adhesives.

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MEANS

[Means for Solving the Problem] The 1st semiconductor device applied to this invention in order to attain the above-mentioned purpose is characterized by joining each aforementioned semiconductor chip mutually in the semiconductor device which has carried out two or more laminatings of the semiconductor chip in which the element was formed by the electric conduction material with which the hole which penetrated and formed the semiconductor substrate of the polar zone of each aforementioned semiconductor chip and the corresponding portion was filled up.
[0007] Thus, by leaving the polar zone, forming a through hole in a semiconductor substrate, and joining the polar zone of each semiconductor chip by the electric conduction material with which this through hole was filled up, the semiconductor device concerning the 1st of the constituted this invention can connect each semiconductor chip electrically, without using a wire, and can join each semiconductor chip mutually.
[0008] If solder or a low melting point metal is used as electric conduction material, while being able to make the electric resistance by junction small, the big junction force is acquired. Moreover, if an electroconductive glue is used as electric conduction material, since heating is not needed, simplification of a process can be attained and the damage by heat, such as an element, etc. can be avoided.
[0009] And in the semiconductor device with which the semiconductor device concerning the 2nd of this invention carried out two or more laminatings of the semiconductor chip in which the element was formed, it is characterized by having connected mutually electrically by the electric conduction material arranged in the through hole in which each aforementioned semiconductor chip makes the polar zone correspond, and has carried out the laminating, and these polar zone penetrated and prepared the polar zone and the semiconductor substrate.
[0010] Thus, also in the semiconductor device concerning the 2nd of the constituted this invention, each semiconductor chip can be connected electrically, without using a wire. Moreover, since the through hole which penetrated the polar zone and the semiconductor substrate is formed, it is possible to bundle up, where the laminating of each semiconductor chip is carried out, and to form a through hole, and simplification of a process can be attained.
[0011] Electric conduction material may be the conductive film formed in the wall surface of a through hole. This conductive film can be formed by depositing the film of conductive metals, such as copper and aluminum, by vacuum evaporationo or plating. Furthermore, each semiconductor chip is mutually joinable by making a through hole fill up with and harden this electroconductive glue, using an electroconductive glue as electric conduction material. And while the touch area of the polar zone of each semiconductor chip and an electroconductive glue increases and being able to make electrical installation more reliable by filling up with an electroconductive glue the opening in which the protective coat on the polar zone of the semiconductor chip located caudad was removed and formed, the junction force between each semiconductor chip can be enlarged.
[0012] In the semiconductor device with which the semiconductor device concerning the 3rd of this invention carried out the laminating of the plurality of the semiconductor chip in which the element was formed moreover, each aforementioned semiconductor chip The aforementioned semiconductor chip which the polar zone is made to correspond, has carried out the laminating, and is located up The aforementioned semiconductor chip which has the through hole formed in the semiconductor substrate of the portion corresponding to the aforementioned polar zone and the bump who penetrated and formed the aforementioned polar zone, and is located caudad The aforementioned polar zone is characterized by what is electrically connected to the aforementioned polar zone of the aforementioned semiconductor chip located up through the aforementioned bump.
[0013] Thus, each semiconductor chip can be connected electrically, without using a wire also in the constituted this invention. And if the polar zone of the semiconductor chip located caudad and the bump of a semiconductor chip located in the upper part are joined by the electroconductive glue, while electric connection can carry out more certainly, each semiconductor chip is mutually joinable.
[0014] The polar zone of the semiconductor chip in which the 1st formed the element of the method of manufacturing the above-mentioned semiconductor device, and the process which forms a through hole in the semiconductor substrate of the corresponding portion, It is characterized by having the process which the aforementioned through hole is covered, and electric conduction material heaps up, and forms the section, and the process which joins each aforementioned semiconductor chip mutually while carrying out the laminating of the plurality of the aforementioned semiconductor chip which has arranged the aforementioned electric conduction material and connecting the aforementioned polar zone mutually electrically. The semiconductor device concerning the 1st of this invention is obtained by this, and while being able to connect mutually

electrically, without carrying out wirebonding of between semiconductor chips, the semiconductor chips which carried out the laminating are joinable.
[0015] Electric conduction material may be a soldering paste. In this case, it can heap up, and can form according to the process which the section covers a through hole and arranges many soldering pastes from the capacity of a hole, and the process which heats the semiconductor chip which has arranged the soldering paste, fuses a soldering paste, and removes the flux in a soldering paste, and junction can be performed by fusing the solder which heated two or more semiconductor chips which carried out the laminating, and has been arranged at the through hole. Namely, if a soldering paste is used, the laminating of the semiconductor chip will be carried out, solder can be performed and solder can join each semiconductor chip automatically with the self-weight of a semiconductor chip heating and by carrying out a reflow at the time of ******. Moreover, when a low melting point metal is used as electric conduction material, if junction is performed by heating and pressurizing the low melting point metal of two or more semiconductor chips which carried out the laminating, it can ensure junction between polar zone, and junction between semiconductor chips. And it becomes possible by using low melting point metals, such as tin and silver, to realize a lead free-lancer.
[0016] The manufacture method of the 2nd semiconductor device concerning this invention is characterized by to have the process which forms the through hole which penetrated the process which the polar zone which defined beforehand the plurality of the semiconductor wafer in_which the element was formed, or a semiconductor chip is made to correspond, and carries out a laminating, and the aforementioned polar zone and the semiconductor substrate of the aforementioned semiconductor wafer or the semiconductor chip which carried out the laminating, and the process which prepare electric-conduction material in the aforementioned through hole, and connect the aforementioned polar zone mutually electrically. Thereby, the semiconductor device concerning the 2nd of this invention can be obtained.
[0017] The electrical installation of the polar zone can form a metal membrane in the wall surface of a through hole by vacuum evaporationo or plating, and can perform it on it. Moreover, when a part of protective coat currently formed on the polar zone is removed and a part of polar zone [at least] has exposed each semiconductor wafer or the semiconductor chip, the electrical installation of each polar zone injects an electroconductive glue into the opening which removed the through hole and the protective coat and was formed, and performs it. Thereby, the touch area of the polar zone and an electroconductive glue can become large, can ensure electrical installation, and can increase the bonding strength between each semiconductor chip.
[0018] The manufacture method of the semiconductor device concerning the 3rd of this invention The process which forms the through hole which penetrated the polar zone of the 1st semiconductor chip, and the semiconductor substrate corresponding to this polar zone, The process which forms the bump who penetrated the polar zone through the through hole formed in the aforementioned polar zone, It is characterized by having the process which arranges the 2nd semiconductor chip in piles and connects electrically the polar zone of the 2nd semiconductor chip of the above to the non-activity side side of the 1st semiconductor chip of the above through the aforementioned bump at the aforementioned polar zone of the 1st semiconductor chip of the above. Thereby, the semiconductor device concerning the 3rd of this invention can be obtained.
[0019] And the process which arranges an electroconductive glue in the through hole which formed in the semiconductor substrate of the 1st semiconductor chip the process which connects electrically the polar zone of the 1st semiconductor chip and the 2nd semiconductor chip, and on the polar zone of the 2nd semiconductor chip, By arranging and putting the 2nd semiconductor device on the non-activity side side of the 1st semiconductor chip, looking like [the process joined by the electroconductive glue] the 2nd polar zone and bump of a semiconductor chip, and therefore performing them The certainty of electrical installation can be improved and it becomes joinable [semiconductor chips].
[0020]
[Embodiments of the Invention] The gestalt of desirable operation of the semiconductor device concerning this invention and its manufacture method is explained in detail according to an accompanying drawing.
[0021] some semiconductor devices which drawing 1 requires for the gestalt of the 1st operation of this invention -- it is a cross section In drawing 1 , as for the semiconductor device 10 which constitutes the stacked mold MCP, the laminating of the semiconductor chip 12 (12a-12d) of plurality (in the case of an operation gestalt four) has been carried out. And each semiconductor chip 12 has the semiconductor substrate 14 which consists of silicon, and while having formed elements, such as a transistor which is not illustrated in the upper part of the semiconductor substrate 14, and resistance, a capacitor, the polar zone 16 is formed. These polar zone 16 is formed by electric conduction material, such as aluminum and an aluminium alloy, and is electrically connected to elements, such as a transistor, through the wiring (not shown) formed in the semiconductor substrate 14.

[0022] Each semiconductor chip 12 makes the polar zone 16a and 16b defined beforehand correspond, has carried out the laminating, and is electrically connected mutually with the solder 18 whose polar zone 16a and 16b which the adjoining semiconductor chip 12 made correspond is electric conduction material.
[0023] That is, the catching hole (through hole) 20 which penetrated and formed the semiconductor substrate 14 in the polar zone 16a and 16b of the semiconductor substrate 14 and the corresponding portion is formed in other semiconductor chips 12a-12c except 12d of semiconductor chips of a bottom. These catching holes 20 are gradually extended towards a non-activity side side (inferior-surface-of-tongue side of drawing 1) from the side which formed the polar zone 16 which is the active side side of a semiconductor chip 12. And the insulator layer 22 which consists of diacid-ized silicon (SiO2) is formed, and it is made to have not flowed through the solder 18 and the semiconductor substrate 14 which have been arranged in a catching hole 20 directly electrically on the non-activity side of the semiconductor substrate 14, and the wall surface of a catching hole 20. Furthermore, the solder 18 arranged in the catching hole 20 of the semiconductor chip 12 located in the drawing bottom was

projected from the non-activity side of the semiconductor substrate 14, and is joined to the upper surface of the polar zone 16 of the bottom semiconductor chip 12 which adjoins the non-activity side side while having joined to the inferior surface of tongue of the polar zone 16.
[0024] thus, the connection whose each semiconductor chips [12a-12d] polar zone 16a and 16b made to correspond formed the semiconductor device 10 concerning the formed 1st operation gestalt in the semiconductor substrate 14 -- since the solder 18 prepared in the hole 20 connects directly electrically, the wire for connecting each semiconductor chip 12 electrically is not needed, but electrical installation between semiconductor chip 12 can be performed easily And in order not to use the wire which is easy to deform, even if it makes the interval between polar zone 16 small, generating of a short circuit etc. can be lost, and it becomes possible to improve the degree of integration of the element of each semiconductor chip 12. Moreover, since it is not necessary to form a terminal area in the periphery section of each semiconductor chip 12 which carried out the laminating, even if it makes [many] the number of laminatings of a semiconductor chip 12, it is not necessary to make small size of the semiconductor chip located up, and mounting efficiency can be raised.
[0025] Furthermore, a semiconductor device 10 can skip the process which joins a semiconductor chip mutually with adhesives by having joined the polar zone 16 of the semiconductor chip 12 which adjoins through solder 18. And in the gestalt of operation, since the catching hole 20 formed in the semiconductor chip 12 is gradually extended towards the non-activity side side which joins other semiconductor chips, the junction force of solder 18 and the polar zone 16 (for example, the solder 18 of semiconductor chip 12a and polar zone 16 of semiconductor chip 12b) of other semiconductor chips can be enlarged.
[0026] in addition, the polar zone 16 of semiconductor chip 12a located in the best stage of drawing 1 when connecting a semiconductor device 10 to the substrate of a package electrically -- wirebonding -- it carries out by carrying out face down bonding
[0027] In the gestalt of the aforementioned implementation, although the case where electric conduction material was solder 18 was explained, electric conduction material may be the so-called low melting point metals, such as tin and silver, and may be electroconductive glues.
[0028] Drawing 2 forms the polar zone 16 and produces a semiconductor chip 12 while it forms wiring first after forming the element which shows the important section of process drawing explaining the manufacture method of the semiconductor device 10 concerning the gestalt of the 1st operation and which is not illustrated to the semiconductor substrate 14 by the well-known method, as shown in drawing 2 (a). Then, from the rear-face (non-activity side) side of a semiconductor chip 12, wet etching is carried out and the catching hole 20 which penetrates the semiconductor substrate 14 and arrives at the rear face of the polar zone 16 is formed for the semiconductor substrate 14.
[0029] Next, as shown in drawing 2 (b), the insulator layer 22 which covers the non-activity side and catching hole 20 of the semiconductor substrate 14, and consists of diacid-ized silicon (SiO2) by the CVD using the tetrapod ethoxy silane (TEOS) etc. is formed. Furthermore, an insulator layer 22 is covered, the photoresist film 30 is formed, by the photo lithography method, this is exposed and developed, and carries out patterning, a hole 32 is established in an electrode 16 and the corresponding position, and the insulator layer 22 currently formed in the field of the polar zone 16 is exposed.
[0030] Then, the insulator layer 22 to which it etched into by having considered as the mask, and the photoresist film 30 was exposed is removed (refer to drawing 2 (c)). Next, the soldering paste 34 used as electric conduction material is formed in a catching hole 20 using screen printing. in order that this soldering paste 34 may join to the polar zone of other semiconductor chips so that it may mention later -- from a catching hole 20 -- suitably -- ********** -- it prepares like Then, the semiconductor chip 12 which has arranged the soldering paste 34 is put into a reflow furnace, a soldering paste 34 is heated and flux is removed, and as shown in drawing 2 (d), it is made the solder plug 36.
[0031] Next, as shown in drawing 2 (e), the predetermined polar zone 16 is made to correspond, and as a non-activity side turns up, it accumulates the semiconductor chip 12 of the number of requests in which the solder connecting plug 36 was formed on it. And where two or more semiconductor chips 12 are accumulated, it arranges at a reflow furnace, and the solder plug 36 is heated to melting temperature. Thereby, the solder plug 36 is fused and is crushed by the weight of a semiconductor chip 12. Then, if a semiconductor chip 12 is cooled, the semiconductor device 10 which solder 18 connected mutually electrically, and the polar zone 16 of the semiconductor chip 12 of the adjoining upper and lower sides was joined to it with it, and was shown in drawing 1 can be obtained.
[0032] In addition, when the electric conduction material arranged to the catching hole 20 is low melting point metals, such as silver, the reflow process of drawing 2 (d) can be skipped. And when joining two or more piled-up semiconductor chips of each mutually with low melting point metals, such as silver, while heating the semiconductor chip 12 of a bottom in the best stage, or both, the whole semiconductor chip which carried out the laminating is pressurized in the vertical direction. Thereby, while being able to transmit heat to a low melting point metal easily through the semiconductor substrate 14, the polar zone of each semiconductor chip is certainly joinable to a low melting point metal. Furthermore, a heating process can be skipped when an electroconductive glue is used as electric conduction material.
[0033] some semiconductor devices which drawing 3 requires for the gestalt of the 2nd operation -- it is a cross section As for the semiconductor device 40 shown in drawing 3 (a), the laminating of the semiconductor chip 12 (12a-12c) of plurality (it sets in this operation gestalt and is three) has been carried out. Each semiconductor chip 12 is arranged so that an active side side may turn into the drawing 3 bottom, makes the polar zone 42 defined beforehand correspond, and has carried out the laminating. And the metal membrane 46 which is the electric conduction material which has formed the through hole 44 which penetrated the polar zone 42 and the semiconductor substrate 14 of each semiconductor chip 12, and formed the semiconductor device 40 in the wall surface of this through hole 44 by vacuum evaporationo, plating, etc. is formed, and the polar zone 42 of each

semiconductor chip 12 is mutually connected electrically through the metal membrane 46. However, the insulator layers 45, such as a silicon oxide, are formed in the portion from which each semiconductor chip 12 serves as a wall surface of the through hole 44 of the semiconductor substrate 14, and a metal membrane 46, the semiconductor substrate 14, and between are intercepted electrically.

[0034] Thus, the formed semiconductor device 40 can be carried out like drawing 4 , and can be manufactured. First, as shown in Step 60 of drawing 4 , an element, the polar zone, etc. are formed in a semiconductor wafer by the usual method. Then, while turning into request number of sheets (it sets in this operation gestalt and they are three sheets) the semiconductor wafer in which the element etc. was formed and turning an active side up, the polar zone 42 which forms a through hole 44 is made to correspond, and a laminating is carried out (Step 62). Next, where the laminating of the semiconductor wafer is carried out, a laser beam etc. is used for the portion of the polar zone 42, and a through hole 44 is formed (Step 64). You may form this through hole 44 by etching. Moreover, after making a hole by the laser beam since the wall surface of a hole is ruined when forming a through hole 44 using a laser beam, to ********** and operate orthopedically is good.

[0035] Then, as shown in Step 66, an insulator layer 45 is formed in the portion used as the wall surface of the through hole 44 of the semiconductor substrate 14. Formation of this insulator layer 45 heats the semiconductor wafer in which the through hole 44 was formed, in being immersed and an oxidizing atmosphere in concentrated-nitric-acid liquid, oxidizes the through-hole wall surface section of the semiconductor substrate 14, and is SiO2. It carries out. Then, alkali etc. removes the metal oxide film (passive state) currently formed in the polar zone 42.

[0036] Next, as shown in Step 68, a metal membrane 46 is formed in the wall surface of the through hole 44 which formed the insulator layer by vacuum evaporationo, electroless deposition, etc. In addition, when forming a metal membrane 46 by plating, it is good to form ground metals, such as Ti (titanium), by vacuum deposition or CVD, and to form metal membranes, such as copper, by electroless deposition after that.

[0037] If a metal membrane 46 is formed in a through hole 44, it will divide into a chip size using a laser beam, a diamond blade, etc., carrying out the laminating of the semiconductor wafer, as shown in Step 70. Furthermore, the laminate cut to the chip size is mounted in the substrate of a package, a resin seal etc. is performed, and it is made the MCP semiconductor device of a stacked mold (Step 72).

[0038] In addition, after cutting the semiconductor wafer in which an element, the polar zone 42, etc. were formed and forming a semiconductor chip 12, the laminating of the semiconductor chip of the number of requests is carried out, and you may make it form a through hole 44 in the aforementioned operation gestalt, although the case where carried out the laminating of the semiconductor wafer and a through hole 44 was formed was explained.

[0039] drawing 3 (b) -- a part of modification of the 2nd operation gestalt -- it is a cross section Two semiconductor chips 12a and 12b double a non-activity side side, and the laminating of this semiconductor device 50 has been carried out. And the through hole 44 which penetrated the polar zone 42 which each semiconductor chip 12 made correspond, and the semiconductor substrate 14 is formed, the metal membrane 46 is formed in the wall surface of this through hole 44, and the polar zone 42 of each semiconductor chip 12 is electrically connected by the metal membrane 46.

[0040] In addition, it is the same as that of the above to have insulated the wall surface of the through hole 44 of the semiconductor substrate 14 by the insulator layer 45. Moreover, this semiconductor device 50 can be manufactured almost like the case of a semiconductor device 40. Moreover, although the semiconductor device 50 shown in drawing 3 (b) explained the case where two semiconductor chips 12 were piled up, it can carry out the laminating of arbitrary numbers of the semiconductor chips among semiconductor chips 12a and 12b.

[0041] some semiconductor devices which drawing 5 requires for the gestalt of the 3rd operation -- it is a cross section As for the semiconductor device 74 shown in drawing 5 (a), the laminating of the semiconductor chip 76 (76a-76c) of plurality (in the case of an operation gestalt three) has been carried out. And the polar zone 78 and the semiconductor substrate 80 which were formed in each semiconductor chip 76 are penetrated, the through hole 82 is formed, this through hole 82 is filled up with the electroconductive glue 84 which is electric conduction material, it is joined by the electroconductive glue 84 and each semiconductor chip 76 is unified. Moreover, the opening 88 formed by exfoliating in the passivation film 86 as a protective coat which consists of a silicon oxide of the semiconductor chips 76b and 76c located down the drawing etc. is also filled up with the electroconductive glue 84.

[0042] That is, after a semiconductor chip generally forms wiring and the polar zone, it formed the passivation film 86 on it, and has protected wiring etc. And the passivation film 86 located on the polar zone 78 is removed in order to connect with other semiconductor chips, the polar zone of a package substrate, etc. electrically. For this reason, if two or more laminatings of the semiconductor chip are carried out, since the place which removed the passivation film 86 will serve as an opening 88, by filling up the opening 86 with an electroconductive glue 84, and performing electrical installation of each polar zone 78, the touch area of an electroconductive glue 84 and the polar zone 78 is increased, and more positive electrical installation is performed, and the junction force between each semiconductor chip is enlarged.

[0043] It manufactures by carrying out this semiconductor device 74 as following. First, etching etc. removes the passivation film 86 which exists on the polar zone 78 of the semiconductor wafer in which an element, the polar zone 78, etc. were formed, or a semiconductor chip 76, and the polar zone 78 is exposed. Next, the polar zone 78 is made to correspond and two or more laminatings of the semiconductor wafer or semiconductor chip to which the polar zone 78 was exposed are carried out. Then, in the state where the laminating of a semiconductor wafer or the semiconductor chip 76 was carried out, the through hole 82 which penetrated the polar zone 78 and the semiconductor substrate 80 of each semiconductor chip 76 is formed collectively, and the insulator layer which is not illustrated on the wall surface of the breakthrough 82 of the semiconductor substrate 80 is prepared.

Although it can form like the gestalt of the 2nd operation of the above, you may form this insulator layer as follows.
[0044] The semiconductor wafer or semiconductor chip 76 which formed the through hole 82 where a laminating is carried out is put into a CVD system as it is, and a silicon oxide is formed in the wall surface of a through hole 82 by CVD using TEOS etc. At this time, as shown in drawing 6 (a), a silicon oxide 89 is deposited on the top semiconductor wafer or the upper surface of semiconductor chip 76a, and the wall surface of the breakthrough 82 of each semiconductor wafer or semiconductor chips 76a-76c, and is hardly formed in the field which forms the opening 88 formed between each semiconductor wafer or each semiconductor chip 76. Since the passivation film 86 is thin, this has the narrow width of face of the vertical direction of an opening 88, and since the circumference moreover serves as a letter object of sealing, it is because material gas is not supplied to the back of an opening 88.
[0045] Thus, if a silicon oxide 89 is formed, it will ********** extensively from the upper part of the semiconductor wafer with which the silicon oxide 89 was formed, or semiconductor chip 76a, and as shown in drawing 6 (b), the silicon oxide 89 formed by the upper surface of semiconductor wafer or semiconductor chip 76a will be removed. Thereby, the insulator layer which becomes the wall surface of a through hole 82 from a silicon oxide 89 is formed.
[0046] Next, while sealing the lower part of a through hole 82, pressing an electroconductive glue 84 fit from the upper part of a through hole 82 and filling up the interior of a through hole 82 and an opening 88 with an electroconductive glue 84, it is made to arrange and harden so that it may wear on the upper surface of the top polar zone 78. Then, if it is the semiconductor wafer which carried out the laminating to having described above similarly, it divides into a chip size and mounts in a package substrate.
[0047] Drawing 5 (b) shows the modification of the semiconductor device concerning the 3rd operation gestalt. As for this semiconductor device 110, the laminating of the semiconductor chip 112 (112a-112c) has been carried out. The crevice 114 is formed in a part of active side of the semiconductor substrate 80, and, as for each semiconductor chip 112, the polar zone 116 is formed in this crevice 114. For this reason, an opening 118 will be formed in the upper part of the polar zone 116 of a lower semiconductor chip if the laminating of each semiconductor chip 112 is carried out. Moreover, the through hole 82 which penetrated the polar zone 116 and the semiconductor substrate 80 is formed in the center section of the crevice 114. The insulator layer which consists of a silicon oxide etc. and which is not illustrated is formed in the wall surface of this through hole 82. And while having filled up the through hole 82 and the opening 118 with the electroconductive glue 84 and having connected electrically the polar zone 116 of each semiconductor chip 112, the semiconductor chip 112 which adjoins in the vertical direction is joined mutually. The same effect as the above can be acquired also in the semiconductor device 110 of this modification.
[0048] some semiconductor devices which drawing 7 requires for the 4th operation gestalt -- it is a cross section Two semiconductor chips 76a and 76b make the polar zone 78 correspond, and the laminating of the semiconductor device 90 shown in drawing 7 (a) has been carried out. And while having formed the through hole 92 of the shape of a taper gradually extended towards the bottom from which upper semiconductor chip 76a becomes the semiconductor substrate 80 of the lower part of the polar zone 78 a non-activity side side, the through hole 94 smaller than a through hole 92 is formed also in the polar zone 78. Moreover, the stud bump 96 who consists of gold is formed in the polar zone 78. This stud bump 96 has the connection 98 which projected from the soffit of the semiconductor substrate 80, contacted the upper surface of the polar zone 78 of semiconductor chip 76b which the soffit of a connection 98 arranges and fixed to the semiconductor chip 76a bottom, and is connecting electrically each polar zone 78 of both the semiconductor chips 76a and 76b while a part extends under the polar zone 78 through a through hole 94.
[0049] Thus, after the constituted semiconductor device 90 removes the passivation film 86 on the polar zone 78 of semiconductor chip 76a, it **********s the semiconductor substrate 80 and forms a through hole 92. Furthermore, the polar zone 78 of semiconductor chip 76a is **********ed, and a through hole 94 is formed. Then, the capillary tube of wirebonding equipment is arranged on the through hole 94 of the polar zone 78, and the stud bump 96 is formed, pulling out a golden wire. Thereby, as the stud bump 96 showed drawing 7 (a), it projects under the polar zone 78 and a connection 98 is formed. And if the polar zone 78 is made to correspond, semiconductor chips 76a and 76b are piled up and both are fixed with adhesives etc., it will be alike, and more, the stud bump's 96 connection 98 is contacted to the polar zone 78 of downward semiconductor chip 76b, and it connects electrically.
[0050] Drawing 7 (b) shows the modification of the 4th operation gestalt. As for this semiconductor device 100, through holes 92 and 94 are formed in the upper semiconductor substrate 80 and upper polar zone 78 of semiconductor chip 76a. Furthermore, the stud bump 96 is formed in the polar zone 78 at upper semiconductor chip 76a. This stud bump 96 is the connection 98 which the lower part penetrated the polar zone 78 and was projected under the polar zone 78. And the connection 98 is electrically connected to the polar zone 78 of lower semiconductor chip 76b through the electroconductive glue 102. Thus, while being able to make electrical installation more reliable by joining the lower polar zone 78 and the lower stud bump 96 of semiconductor chip 76b using an electroconductive glue 102, semiconductor chips 76a and 76b are mutually joinable. In addition, the insulator layer which is not illustrated is prepared in the wall surface of a through hole 92.
[0051] Thus, the semiconductor device 100 of constituted drawing 7 (b) forms the stud bump 96 in the electrode section 78 of semiconductor chip 76a used as the bottom like the above. A soffit projects and bends from the undersurface of the semiconductor substrate 80, and this stat bump 96 makes it the size of a grade. Moreover, semiconductor chip 76b used as the bottom arranges the electroconductive glue 102 of a proper quantity on the electrode section 78, after removing the passivation film 86 on the electrode section 78. And semiconductor chip 76a is arranged in piles on semiconductor chip 76b, and the electrode section 78 of both the semiconductor chips 76a and 76b is electrically connected through an electroconductive glue

102 and the stud bump 96.
[0052] Drawing 7 (c) shows other examples of the through hole formed in a semiconductor substrate. The active side side in which the electrode section 78 was formed serves as the straight hole 106 which has the wall surface which intersected perpendicularly with the field of the semiconductor substrate 80, and this through hole 104 serves as the expansion hole 108 which the non-activity side side of the semiconductor substrate 80 extended gradually towards the non-activity side.
[0053] Thus, if the through hole 104 of the shape of a funnel which consists of a straight hole 106 and an expansion hole 108 is formed, when the semiconductor substrate 80 is thick, it can prevent opening in the non-activity side of a through hole 104 becoming larger than required, and risk (it connects) of contacting the electrode section which adjoined the electrode section of an upper semiconductor chip and the electrode section of a corresponding bottom semiconductor chip can be avoided. Furthermore, when the electrode section 78 approaches and is prepared, it can prevent that the adjoining through holes are connected on the way. Moreover, as for the funnel-like through hole 104, when filled up with electric conduction material, the whole can lessen the fill of electric conduction material as compared with the through hole currently formed in the shape of a taper. And when carrying out the laminating of the semiconductor chip in which bumps, such as a stud bump, were formed on the electrode section 78, the alignment of a bump and a through hole, i.e., the alignment of a semiconductor chip which carries out a laminating, can be performed easily.
[0054] This through hole 104 can be formed as follows.
[0055] First, wet etching of the semiconductor substrate 80 is carried out from a non-activity side side, and the expansion pore 108 is formed. If predetermined-time etching is carried out and the expansion pore 108 is formed, a semiconductor chip 76 will be washed, it will dry, a laser beam will be irradiated from a non-activity side side, and the straight hole 106 will be formed. In addition, after forming the straight hole 106, you may perform the plastic surgery which carries out wet etching and smooths the wall surface of a through hole 104. Moreover, the through hole 94 of the electrode section 78 is formed like the above. And you may form a parallel bore 106 by the dry etching which used plasma. Furthermore, the parallel bore 106 which penetrated the body substrate 80 first is formed by the laser beam or plasma etching, and you may make it form the expansion hole 108 by wet etching after that.

[Translation done.]

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DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]
[Drawing 1] some semiconductor devices concerning the gestalt of the 1st operation of this invention -- it is a cross section
[Drawing 2] It is important section process drawing explaining the operation gestalt of the manufacture method of the semiconductor device concerning the 1st operation gestalt.
[Drawing 3] some semiconductor devices concerning the gestalt of the 2nd operation of this invention -- it is a cross section
[Drawing 4] It is a flow chart explaining the operation gestalt of the manufacture method of the semiconductor device concerning the 2nd operation gestalt.
[Drawing 5] some semiconductor devices concerning the 3rd operation gestalt of this invention -- it is a cross section
[Drawing 6] It is drawing explaining how to form an insulator layer in the wall surface of the through hole of the semiconductor wafer which carried out the laminating, or a semiconductor chip.
[Drawing 7] It is the cross section showing the example of everything but the through hole formed in a semiconductor substrate of the semiconductor device concerning the 4th operation gestalt of this invention with a cross section in part.
[Description of Notations]
10 Semiconductor Device
12a-12d Semiconductor chip
14 80 Semiconductor substrate
16, 16a-16c Polar zone
18 Electric Conduction Material (Solder)
20 Through Hole (Catching Hole)
34 Electric Conduction Material (Soldering Paste)
36 Solder Plug
40 50 Semiconductor device
42 78 Polar zone
44 82 Through hole
45 Insulator Layer
46 Electric Conduction Material (Metal Membrane)
76a-76c Semiconductor chip
84 Electric Conduction Material (Electroconductive Glue)
88,118 Opening
89 Silicon Oxide
90,100 Semiconductor device
92 94,104 Through hole
96 Stat Bump
102 Electroconductive Glue
110 Semiconductor Device
112a-112c Semiconductor chip
116 Polar Zone

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CORRECTION or AMENDMENT

[Official Gazette Type] Printing of amendment by the convention of 2 of Article 17 of patent law.
[Section partition] The 2nd partition of the 7th section.
[Date of issue] February 14, Heisei 15 (2003. 2.14)

[Publication No.] JP,2001-60654,A (P2001-60654A)
[Date of Publication] March 6, Heisei 13 (2001. 3.6)
[**** format] Open patent official report 13-607.
[Filing Number] Japanese Patent Application No. 11-234577.
[The 7th edition of International Patent Classification]

H01L 25/065
25/07
25/18

[FI]

H01L 25/08 B

[Procedure revision]
[Filing Date] November 11, Heisei 14 (2002. 11.11)
[Procedure amendment 1]
[Document to be Amended] Specification.
[Item(s) to be Amended] Claim.
[Method of Amendment] Change.
[Proposed Amendment]
[Claim(s)]
[Claim 1] The semiconductor device characterized by joining each aforementioned semiconductor chip mutually by the electric conduction material with which the hole which penetrated and formed the semiconductor substrate of the electrode section of each aforementioned semiconductor chip and the corresponding portion in the semiconductor device which has carried out two or more laminatings of the semiconductor chip in which the element was formed was filled up.
[Claim 2] The aforementioned electric conduction material is a semiconductor device according to claim 1 characterized by being solder or a low melting point metal.
[Claim 3] The aforementioned electric conduction material is a semiconductor device according to claim 1 characterized by being an electroconductive glue.
[Claim 4] It is the semiconductor device characterized by having connected mutually electrically by the electric conduction material arranged in the through hole in which each aforementioned semiconductor chip made the electrode section correspond, and had carried out the laminating, and these electrode sections penetrated the electrode section and the semiconductor substrate in the semiconductor device which carried out two or more laminatings of the semiconductor chip in which the element was formed, and prepared.
[Claim 5] The aforementioned electric conduction material is a semiconductor device according to claim 4 characterized by being the conductive film formed in the wall surface of the aforementioned through hole.
[Claim 6] The aforementioned electric conduction material is a semiconductor device according to claim 4 characterized by being the electroconductive glue with which the aforementioned through hole was filled up.
[Claim 7] The aforementioned electroconductive glue is a semiconductor device according to claim 6 characterized by being filled up with the opening in which the protective coat on the aforementioned electrode section of the aforementioned semiconductor chip located below was removed and formed.
[Claim 8] In the semiconductor device which carried out the laminating of the plurality of the semiconductor chip in which the element was formed
Each aforementioned semiconductor chip makes the electrode section correspond, and has carried out the laminating.

The aforementioned semiconductor chip located up has the through hole formed in the semiconductor substrate of the portion corresponding to the aforementioned electrode section, and the bump who penetrated and formed the aforementioned electrode section.
The aforementioned semiconductor chip located below is electrically connected to the aforementioned electrode section of the aforementioned semiconductor chip in which the aforementioned electrode section is located up through the aforementioned bump.
The semiconductor device characterized by things.
[Claim 9] The aforementioned electrode section of the semiconductor chip located in the aforementioned lower part and the aforementioned bump of a semiconductor chip located in the aforementioned upper part are a semiconductor device according to claim 8 characterized by having joined by the electroconductive glue.
[Claim 10] The electrode section of the semiconductor chip in which the element was formed, and the process which forms a through hole in the semiconductor substrate of the corresponding portion,
The process which the aforementioned through hole is covered, and electric conduction material heaps up, and forms the section,

The process which joins each aforementioned semiconductor chip mutually while carrying out the laminating of the plurality of the aforementioned semiconductor chip which has arranged the aforementioned electric conduction material and connecting the aforementioned electrode section mutually electrically,
The manufacture method of the semiconductor device characterized by ****(ing).
[Claim 11] The aforementioned electric conduction material is a soldering paste.
The aforementioned peak raising section is formed according to the process which covers the aforementioned through hole and arranges many soldering pastes from the capacity of a hole, and the process which heats the aforementioned semiconductor chip which has arranged the soldering paste, fuses a soldering paste, and removes the flux in a soldering paste.
The aforementioned junction is performed by fusing the solder which heated two or more aforementioned semiconductor chips which carried out the laminating, and has been arranged at the aforementioned through hole.
The manufacture method of the semiconductor device according to claim 10 characterized by things.
[Claim 12] The process which the electrode section which defined beforehand the plurality of the semiconductor wafer in which the element was formed, or a semiconductor chip is made to correspond, and carries out a laminating,
The process which forms the through hole which penetrated the aforementioned electrode section and the semiconductor substrate of the aforementioned semiconductor wafer or semiconductor chip which carried out the laminating,
The process which prepares electric conduction material in the aforementioned through hole, and connects the aforementioned electrode section mutually electrically,
The manufacture method of the semiconductor device characterized by ****(ing).
[Claim 13] A part of protective coat currently formed on the aforementioned electrode section is removed, and a part of aforementioned electrode section [at least] has exposed each aforementioned semiconductor wafer or the aforementioned semiconductor chip.
The electrical installation of each aforementioned electrode section is carrying out by injecting an electroconductive glue into the opening which removed the aforementioned through hole and the aforementioned protective coat, and was formed.
The manufacture method of the semiconductor device according to claim 12 made into ******.
[Claim 14] The process which forms the through hole which penetrated the semiconductor substrate corresponding to the 1st electrode section and this electrode section of a semiconductor chip,
The process which forms the bump who penetrated the electrode section through the through hole formed in the aforementioned electrode section,
The process which arranges the 2nd semiconductor chip in piles and connects electrically the electrode section of the 2nd semiconductor chip of the above to the non-activity side side of the 1st semiconductor chip of the above through the aforementioned bump at the aforementioned electrode section of the 1st semiconductor chip of the above,
The manufacture method of the semiconductor device characterized by ****(ing).
[Claim 15] The process which connects electrically the electrode section of the 1st semiconductor chip of the above, and the 2nd semiconductor chip of the above,
The process which arranges an electroconductive glue in the through hole formed in the semiconductor substrate of the 1st semiconductor chip of the above, and on the aforementioned electrode section of the 2nd semiconductor chip of the above,
The process which arranges and puts the 2nd semiconductor device of the above on the non-activity side side of the 1st semiconductor chip, and joins the electrode section and the aforementioned bump of the 2nd semiconductor chip of the above by the aforementioned electroconductive glue,
The manufacture method of the semiconductor device according to claim 14 characterized by ****(ing).

[Translation done.]

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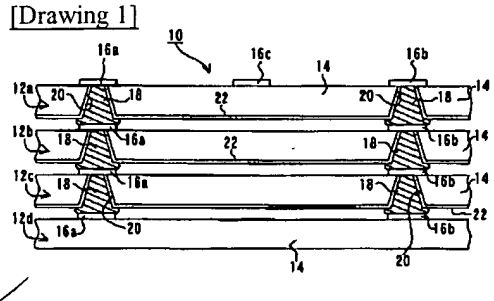
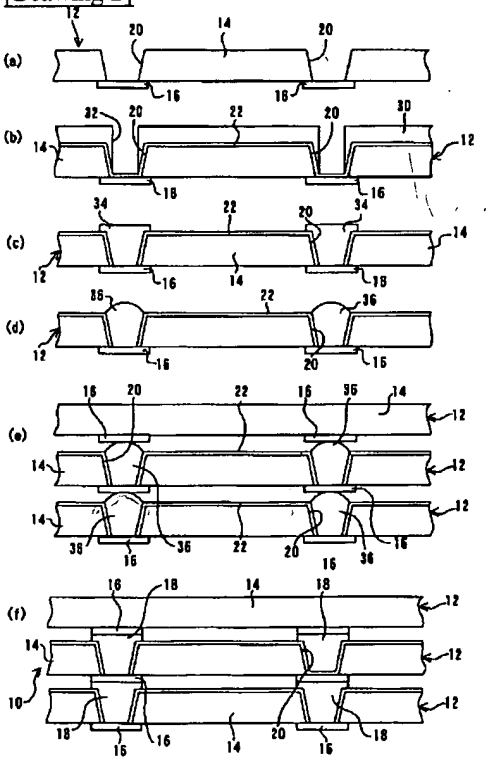
DRAWINGS

[Drawing 1]

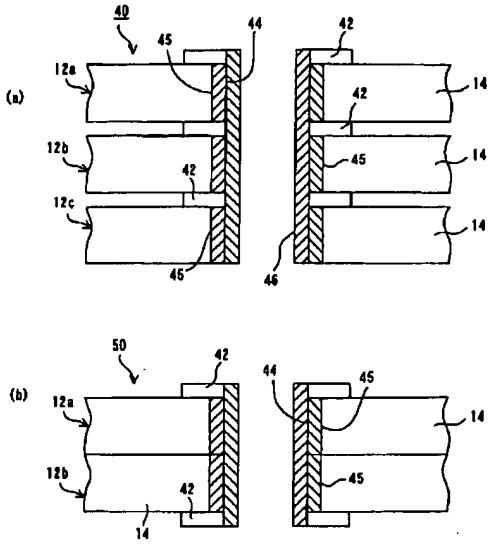


10:半導体装置　16a～16d:電極部
12a～12d:半導体チップ　18:半田
14:半導体基板　20:接続穴

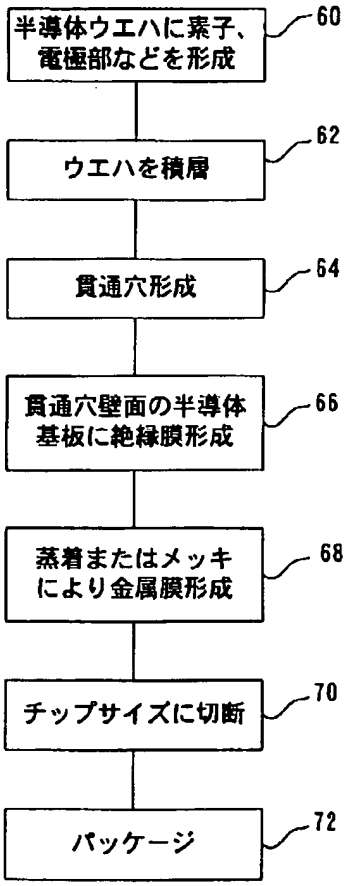
[Drawing 2]



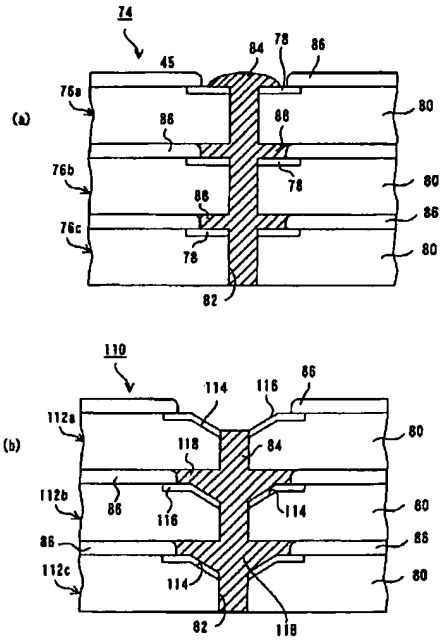
[Drawing 3]



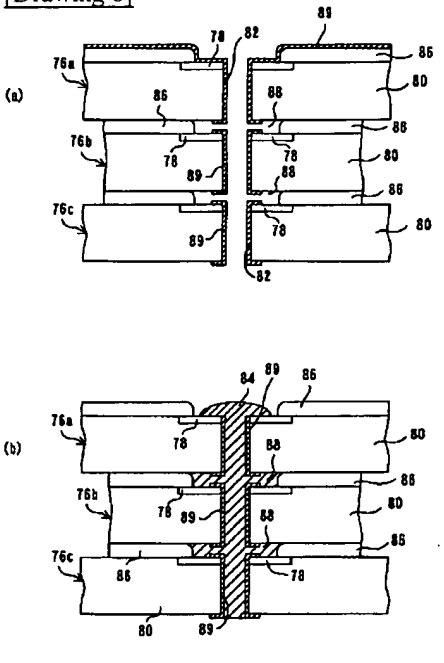
[Drawing 4]



[Drawing 5]

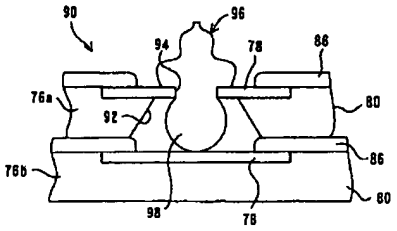


[Drawing 6]

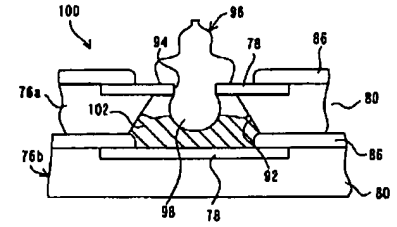


[Drawing 7]

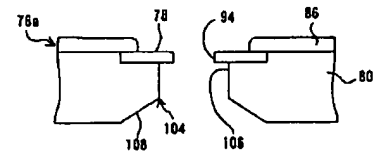
(a)



(b)



(c)



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